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Title of the Invention : SEMICONDUCTOR DEVICE

(Page 2, left column, line 22 – right column, line 4)

【0002】

【Prior Art】 In circuit boards fabricated today, noises are generated due to various causes. Such noises adversely affect the operation of a circuit, thereby causing malfunction of the circuit. With respect to this problem, when designing a circuit, as a measure to prevent noises generated in a circuit board, a circuit designer makes a circuit in which a bypass capacitor is inserted in the vicinity of a semiconductor device. The bypass capacitor is intended to be inserted between a ground potential part and a power supply potential part in a semiconductor device. Being highly effective in preventing noises generated in a circuit board, the bypass capacitor is in common and frequent use. Components to be mounted that can be used as the capacitor are categorized into a type intended to be inserted, a type intended to be surface-mounted and the like. Such capacitors include a ceramic capacitor, a tantalum electrolytic capacitor and the like. Furthermore, a ceramic multilayer wiring board may include a layer having a capacitance generating region. According to this mode, the number of electronic components on a wiring board can be reduced, and a component cost can be reduced. Furthermore, a component-mounted surface of the

wiring board can be used effectively. Therefore, in a ceramic multilayer wiring board, the use of a circuit board housing a capacitor also has been on its way to becoming common. FIG. 2 is a view in cross section of an example of a conventional semiconductor device housing a capacitor.

【0003】 In a semiconductor device 21 shown in FIG. 2, a bypass capacitor is formed in the following manner. That is, a capacitance generating region that is made up of an inner layer electrode 26 and a dielectric 27 is formed between via holes 25 in an inner portion of a ceramic substrate 23 provided with a semiconductor element 22 and electrodes 24. According, for example, to the method suggested in JP 4(1992)–280496 A, a desired via is formed in a green sheet of a ceramic composition and is filled with a conductive paste. An inner layer electrode pattern is printed on the sheet by screen printing using a conductive paste, and a dielectric paste is applied by screen printing so as to cover a wiring pattern. A printed product thus obtained is dried, and subsequently, the inner layer electrode 26 is printed on a dielectric-formed portion using a conductive paste. This process is performed repeatedly so that a conductive layer and a dielectric layer are formed alternately, thereby forming a capacitance generating region.